Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A power device, comprising:

a semiconductor substrate of first conductivity having an upper surface and a lower surface;

a first electrode terminal coupled to a first conductive region provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

a second electrode terminal coupled to a second conductive region provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface;

a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region, and completely surrounded by the isolation diffusion region, and formed proximate the first surface of the isolation diffusion region; and

a passivation layer provided over the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region, the passivation layer comprising a polyimid layer and an oxide layer;

wherein the peripheral junction region is different than the first conductive region and the second conductive region, and the peripheral junction region is in direct contact with the oxide layer, and

wherein the first electrode terminal and the second electrode terminal define a vertical electrical current path therebetween.

2. (original) The device of claim 1, wherein the peripheral junction region is a P+ region and the isolation diffusion region is a P region.

3. (previously presented) The device of claim 1, wherein the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region.

Claims 4-25. (canceled)

26. (currently amended) The device of claim 1, wherein the oxide layer [[and]] contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region.

Claim 27. (canceled)

28. (previously presented) The device of claim 1, wherein the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region.

Claim 29. (canceled)

30. (currently amended) The device of claim 1, wherein the device is a diode and the first electrode terminal is spaced ~~space~~ apart from the isolation diffusion region.

31. (new) A power semiconductor device comprising:

a semiconductor substrate of first conductivity type having an upper surface and a lower surface;

a first region disposed proximate the upper surface of the substrate;

a first electrode disposed on the upper surface of the substrate and electrically coupled to the first region;

a second region of second conductivity type proximate the lower surface of the substrate;

a second electrode disposed on the lower surface of the substrate and electrically coupled to the second region;

an isolation diffusion region of second conductivity type provided at a periphery of the substrate and extending from the upper surface of the substrate to the lower surface of the substrate;

a peripheral junction region of second conductivity type disposed adjacent the upper surface and formed at least partly within the isolation diffusion region, the isolation region completely surrounding the peripheral junction region at the periphery of the substrate;

a layer of silicon dioxide disposed over the upper surface of the substrate overlying at least the isolation region, the peripheral junction region and at least some of the upper surface of the substrate;

a layer of polyimide overlying the layer of silicon dioxide;

wherein the peripheral junction region is spaced apart from the first conductive region and the second conductive region, but is in direct contact with the silicon dioxide layer, and

wherein the first electrode terminal and the second electrode terminal define a vertical electrical current path therebetween.

32. (new) A power semiconductor device as in claim 31 wherein the first electrode comprises a cathode and the second electrode comprises an anode.

33. (new) A power semiconductor as in claim 32 wherein the first conductivity type is n conductivity type and the second conductivity type is p conductivity type.

34. (new) A power semiconductor as in claim 31 wherein the first region is first conductivity type.

35. (new) A power semiconductor as in claim 31 wherein the first region is second conductivity type.

36. (new) A power semiconductor as in claim 31 wherein the first region includes a lower portion of second conductivity type and an upper portion of first conductivity type.